104 to clamp voltages between terminals 102, 104 from ESD events when the voltage at the higher voltage terminal 102 exceeds the voltage at the lower voltage terminal 104 by more than a transient triggering voltage and/or a DC breakdown voltage for the protection circuitry 108.

FIG. 3 illustrates, in cross-section, a semiconductor device structure 200 suitable for use as the protection circuitry 108 and/or BJT element 120 in the electronic device 100 of FIG. 1 in accordance with one or more exemplary embodiments. The protection device structure 200 includes a BJT element (e.g., BJT element 120) having a collector region (comprised of regions 214, 250) and an emitter region (comprised of region 252) having the same conductivity and a base region (comprised of regions 212, 242, 254) of the opposite conductivity formed in a substrate 201 of semiconductor material. As described above in the context of FIG. 1, in exemplary embodiments, the collector regions 214, 250 are coupled to a first package interface 272 corresponding to a higher voltage terminal 102 of the electronic device 100 while the emitter region 252 and the base regions 212, 242, 254 are electrically connected to one another and coupled to a second package interface 274 corresponding to a lower voltage terminal 104 of the electronic device 100.

The emitter region 252 is relatively shallow and is formed in or otherwise resides within a base well region 242 having an opposite conductivity type as the emitter region 252. The base well region 242 has a dopant concentration that is greater than a dopant concentration of a surrounding base well region 212, and accordingly, the base well region 242 may be alternatively referred to herein as being higher (or heavier) doped and the base well region 212 may be referred to herein as lower (or lighter) doped. As described below in the context of FIG. 8, the lighter doped base well region 212 may be comprised of one or more different regions having a dopant concentration less than the dopant concentration of the higher doped base well region 242. A collector well region 214 having the same conductivity type as the emitter region 252 and an opposite conductivity type as the base regions 212, 242, 254 extends from the upper surface of the substrate 201 to a depth that is greater than a depth of the emitter region 252. In this regard, the collector well region 214 pulls the breakdown region within the portion of the base well regions 212, 242 residing between the collector well region 214 and the emitter region 252 deeper and away from the upper surface of the protection device structure 200.

In accordance with one or more embodiments, the collector well region 214 also extends to a depth relative to the surface of the substrate 201 that is greater than a depth of the higher doped base well region 242. In the illustrated embodiment of FIG. 3, the depth of the collector well region 214 relative to the upper surface of the substrate 201 is less than or equal to the depth of the lighter base region 212. In this regard, a portion of the lighter doped base region 212 underlies the collector regions 214, 250 (or alternatively, the collector regions 214, 250 overlie a portion of the lighter doped base region 212). In other words, the collector well region 214 does not underlie the lighter doped base region 212. In accordance with one or more embodiments, the depth of the emitter region 252 is in the range of about 0.3 microns to about 0.6 microns, the depth of the higher doped base well region 242 is in the range of about 1.5 microns to about 2 microns, and the depth of the collector well region 214 is about 4 microns. In the illustrated embodiment, the substrate 201 is realized as a silicon-on-insulator (SOI) substrate that includes a buried layer of dielectric material 204 overlying a handle layer of semiconductor material 202, wherein the portion of the lighter doped base region 212 underlying the collector regions 214, 250 resides between the dielectric material 204 and the collector well region 214. It should be noted that the subject matter described herein is not limited to SOI substrates, and the protection device structure 200 may also be fabricated on a bulk semiconductor substrate.

In exemplary embodiments, isolation regions 228, 230, 232, 234 of dielectric material 225 are formed in the upper surface of the substrate 201 such that an isolation region 230 resides laterally between the emitter region 252 and the collector contact region 250 and another isolation region 232 resides laterally between the emitter region 252 and the base contact region 254. In exemplary embodiments, the isolation regions 228, 230, 232, 234 are realized as shallow isolation regions having a depth that is greater than the depths of the contact regions 250, 252, 254 but less than the depths of the collector well region 214 and the higher doped base well region 242. As described in greater detail below, the isolation region 230 encourages distribution of the collector voltage (e.g., at terminal 272) vertically through a greater percentage (or area) of the base well regions 212, 242 while the isolation region 232 encourages distribution of the collector voltage laterally across a greater percentage (or area) of the base well regions 212, 242 underlying the base contact region 254 and/or otherwise distal to the collector well region 214.

In the illustrated embodiment of FIG. 3, the proximal lateral boundaries of the collector well region 214 and the higher doped base well region 242 extend underneath the shallow isolation region 230 to define a breakdown region within the portion of the lighter doped base region 212 that underlies the shallow isolation region 230 and resides between the collector well region 214 and the higher doped base well region 242. In exemplary embodiments, the collector well region 214 and the higher doped base well region 242 are spaced apart by a lateral separation distance 280 corresponding to the width of the portion of the lighter doped base region 212 underlying the shallow isolation region 230 between well regions 214, 242. In this regard, the separation distance 280 dictates the DC breakdown and transient triggering voltages of the protection device structure 200. In accordance with one or more embodiments, the separation distance 280 is about one micrometer (or micron) or less. In some embodiments, the separation distance 244 may be equal to zero, such that the collector well region 214 abuts the base well region 242.

Still referring to FIG. 3, as described above, the isolation region 232 between the emitter region 252 and the base contact region 254 extends to a depth that is greater than the depth of the regions 252, 254 to encourage vertical and lateral distribution of the voltage (or electrical potential) of the collector well region 214 across a greater percentage (or area) of the higher doped base well region 242 and away from the emitter region 252 when the emitter region 252 and the base contact region 254 are electrically connected (or short-circuited) at the same electrical potential, thereby increasing the effective width of the depletion region within the higher doped base well region 242. Additionally, by virtue of the depth of the collector well region 214 being less than the depth of the lighter doped base region 212, at least a portion of the voltage (or electrical potential) of the collector well region 214 may be distributed or otherwise supported by the underlying portion of the lighter doped base region 212. In this manner, the holding voltage of the protection device structure 200 is increased, which, in turn,